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EXAMINER	
DICKEY, THOMAS L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,961	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-140* is/are pending in the application.

4a) Of the above claim(s) *89-94,96-105 and 115* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *88,95,106-109,111-114,116-123 and 125-140* is/are rejected.

7)☒ Claim(s) *110 and 124* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments filed on 06/25/2009 and 09/08/2009 have been entered.

Claim Objections

2. Applicants are advised that should claim 135 be found allowable, claim 136 will be objected to under 37 CFR 1.75 as being an exact duplicate thereof. Likewise, should claim 138 be found allowable, claim 140 will be objected to under 37 CFR 1.75 as being an exact duplicate thereof. When two claims in an application are duplicates, it is proper after allowing one claim to object to the other as being a duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 88, 95, 116-119, and 129-137 are rejected under 35 U.S.C. 102(b) as being anticipated by MATSUNAMI (5,463,246).

With regard to claims 88, 95, 129, 132, 135, and 136, Matsunami discloses an integrated circuit structure comprising a first substrate 11 comprising a first surface

having interconnect contacts 12; and a thinned (to about 50 microns), substantially flexible second substrate 1 completely overlapping the first substrate 11 and comprising a first surface and a second surface at least one of which has interconnect contacts 3, wherein the second surface is opposite the first surface and wherein the second surface of the second substrate 1 is polished; and conductive paths 15 between the interconnect contacts 12 of the first surface of the first substrate 11 and said one of the first surface of the second substrate 1 and the second surface of the second substrate 1; wherein the first surface of the first substrate 11 and one of the first surface of the second substrate 1 and the second surface of the second substrate 1 are bonded in a stacked relationship, the first substrate 11 overlapping at least a majority of the second substrate 1, wherein the second substrate 1 comprises a low stress (thermal) silicon dioxide dielectric layer 2; at least one additional thinned substrate (as seen in figure 4) having circuitry formed thereon; a first of said at least one additional thinned substrate being bonded to the second substrate 1 and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrate 1s and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure. Note figures 2-4, column 6 lines 4-67, and column 7 lines 1-60 of Matsunami.

With regard to claims 116, 117, 119, 130, 133, and 137, Matsunami discloses an integrated circuit structure comprising a first substrate having topside and bottomside surfaces, wherein the topside surface of the first substrate has interconnect contacts; a

thinned (to about 50 microns), substantially flexible second substrate completely overlapping the first substrate and having topside and bottomside surfaces, wherein at least one of the topside surface and the bottomside surface of the second substrate has interconnect contacts, and wherein the bottomside surface of the second substrate is polished; wherein a major portion of the topside surface of the first substrate and one of the topside surface of the second substrate and the bottomside surface of the second substrate are bonded in a stacked relationship; and conductive paths between the interconnect contacts on the topside surface of the first substrate and said one of the topside surface of the second substrate and the bottomside surface of the second substrate, the conductive paths providing electrical connections between the first substrate and the second substrate; wherein the first substrate overlaps at least a majority of the second substrate, wherein at least one of the first and second substrates comprises a low stress silicon dioxide dielectric layer, selected ones of said interconnect contacts of said topside surface of said first substrate are in electrical contact with selected ones of the interconnect contacts of said bottomside surface of said second substrate so as to form said electrical connections; and further comprising: at least one additional thinned substrate having circuitry formed thereon; a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each

additional thinned substrate and at least one of said substrates of the integrated circuit structure.

The applicant's claims 135-137 do not distinguish over the Matsunami reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is relevant, not the recited functions of causing the low stress dielectric laver to have a stress of about 5 x 10^2 dynes/cm^2 or less.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip

opinion[1], page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("'[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that Matsunami's device is capable (when or if stress is applied) of causing the low stress dielectric laver to have a stress of about 5 x 10^2 dynes/cm^2 or less, because a comparison of Applicant's specification to Matsunami's disclosure reveals that Matsunami discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of causing the low stress dielectric laver to have a stress of about 5 x 10^2 dynes/cm^2 or less.

Because it is reasonable to predict that assume that Matsunami's device is capable of performing the claimed function, the burden shifts to Applicants to come forward with

[1] Available at the BPAI website as http://www.uspto.gov/web/offices/dcom/bpai/prec/fd074423.pdf

evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

With regard to claims 118, 131, and 134, Matsunami discloses an integrated circuit structure comprising a first substrate having a first and second surface; a second substrate having a first and second surface, wherein said second surfaces of the first and second substrates are opposite to said first surfaces; wherein at least one of the first substrate and the second substrate is thinned to form at least one thinned (to about 50 microns), substantially flexible substrate and wherein the second surface of the at least one thinned, substantially flexible substrate is polished; wherein the first surface of the first substrate and a major portion of one of the first surface of the second substrate and the second surface of the second substrate are bonded in a stacked relationship by at least one bond, wherein the at least one bond secures a major portion of the second substrate to the first substrate; and conductive paths between at least two of the first surface of the first substrate and the first and second surfaces of the second substrate, wherein the first substrate overlaps at least a majority of the second substrate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 106-108, 111-114, 120-122, 125-128, and 138-140 are rejected under 35 U.S.C.§ 103(a) as obvious over Matsunami (U.S. Patent No. 5,463,246) in view of Leedy (U.S. Patent No. 5,354,695), Faris (U.S. Patent No. 5,786,629) and Sakui et al. (U.S. Patent No. 5,615,163).

In regard to claims 106, 120, and 139 Matsunami discloses the elements of 106, 120, and 139 (as explained above with regard to claims 88 and 116) except the following:

a) at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry (including redundant memory circuitry) formed thereon.

In regard to claims 138 and 140, Matsunami the elements of claim 118 (from which claim 138 and its duplicate or "redundant" claim 140 depend) but not memory circuitry (including redundant memory circuitry) formed thereon.

However, Faris discloses at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry (including redundant[2] memory circuitry) formed thereon (For Example: See Column 3 Lines 60-63, Column 7 Lines 8-13 and Column 12 Lines 5-10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

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[2] "redundant" means "duplicated or added as a precaution against failure, error, etc." See *Collins English Dictionary* (2000). Using circuitry as a precaution against failure is nothing more or less than a recital of intended use of said circuitry. In the context of the claimed device, "redundant" must therefore mean "duplicated", i.e. more than one copy of the disclosed circuitry. Faris discloses more than one copy, thereby disclosing "redundant" circuitry.

semiconductor device of Matsunami to include at least one controller substrate having logic circuitry formed thereon and at least one memory substrate having memory circuitry formed thereon as disclosed in Faris because it aids in providing parallel data processors (For Example: See Column 3 Lines 60-63).

Additionally, since Matsunami and Faris are both from the same field of endeavor, the purpose disclosed by Faris would have been recognized in the pertinent art of Matsunami.

b) a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines.

However, Sakui et al. ("Sakui") discloses a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couple the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines (For Example: See Figure 10, Column 5 Lines 20-67 and Column 6 Lines 1-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines as disclosed in Sakui

because it aids in providing a means for saving the efficiency of a defective bit (For Example: See Column 5 Lines 11-18 and Column 6 Lines 40-63).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

c) a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment.

However, Sakui discloses a gate line selection circuit (22, 23, 24 and 22') that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment as disclosed

in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

d) controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

However, Sakui discloses controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 107 and 121, Matsunami fails to disclose the following:

a) the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 108 and 122, Matsunami fails to disclose the following:

a) programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 111 and 125, Matsunami fails to disclose the following:

a) logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

However, Sakui discloses logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 112 and 126, Matsunami fails to disclose the following:

a) the controller substrate logic is further configured to: prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include that

the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 113 and 127, Matsunami fails to disclose the following:

a) the controller substrate logic is further configured to prevent the use of at least one defective gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

In regards to claims 114 and 128, Matsunami fails to disclose the following:

a) the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

However, Sakui discloses that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Matsunami and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Matsunami.

B. Claims 109 and 123 are rejected under 35 U.S.C. 103(a) as obvious over Matsunami (U.S. Patent No. 5,753,536) in view of Leedy (U.S. Patent No. 5,354,695), Faris (U.S. Patent No. 5,786,629), Sakui et al. (U.S. Patent No. 5,615,163) and Daberko (U.S. Patent No. 5,787,445).

In regards to claims 109 and 123, Matsunami fails to disclose the following:

a) the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

However, Daberko discloses that the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell (For Example: See Abstract, Column 3 Lines 66 and 67, Column 4 Lines 1-11, Column 5 Lines 63-67 and Column 6 Lines 1-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Matsunami to include that an array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell as disclosed in Daberko because it aids in providing direct manipulation of data segments (For Example: See Column 3 Lines 60-64).

Additionally, since Matsunami and Daberko are both from the same field of endeavor, the purpose disclosed by Daberko would have been recognized in the pertinent art of Matsunami.

Allowable Subject Matter

6. Claims 110 and 124 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 88, 95, 106-109, 111-114, 116-123, and 125-140 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thomas L Dickey/
Primary Examiner, Art Unit 2826